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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,866	10/16/2003	Chung Long Chang	24061. / TSMC2002-1305	7401
42717	7590	09/08/2005	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			CRANE, SARA W	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/686,866

Applicant(s)

CHANG ET AL.

Examiner

Sara W. Crane

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-13 and 19-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-13 and 19-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3 February 2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 7 and 8, "a direction perpendicular to the first and second electrodes" is not clear. The first and second electrodes are three dimensional features, and would thus have directions perpendicular to various parts of the electrode. For example, if the electrode is shaped like a pizza box, there would be six directions perpendicular to the electrode, one along a +x direction, one along a -x direction, one along a +y direction, one along a -y direction, one along a +z direction, and one along a -z direction. Is the claim language intended to encompass all of these directions? Or is the intention to specify a top or plan view? Also, "a perimeter" is not clear. How could there be more than one perimeter associated with any particular viewing direction? How is one to identify "a" perimeter"?

Claims 2-13 and 19-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In each of the independent claims, "via" is unclear. Applicant quotes two definitions of this term in the Remarks of 22 June 2005. The first of these definitions states that a via is "to provide vertical connection between stacked up interconnect

metal lines." These claims do not set forth any stacked up interconnect metal lines. Rather, the claim language seems to be using the term "via" specifically to describe a vertical connection between a capacitor electrode and a single interconnect metal line. See, for example, the last three lines of claim 4. So if one is to adopt the first of the two definitions quoted in the Remarks (which the Remarks argue at length should be done), then the pending claims are not clear because the usage of the term "via" in these claims does not comply with the definition.

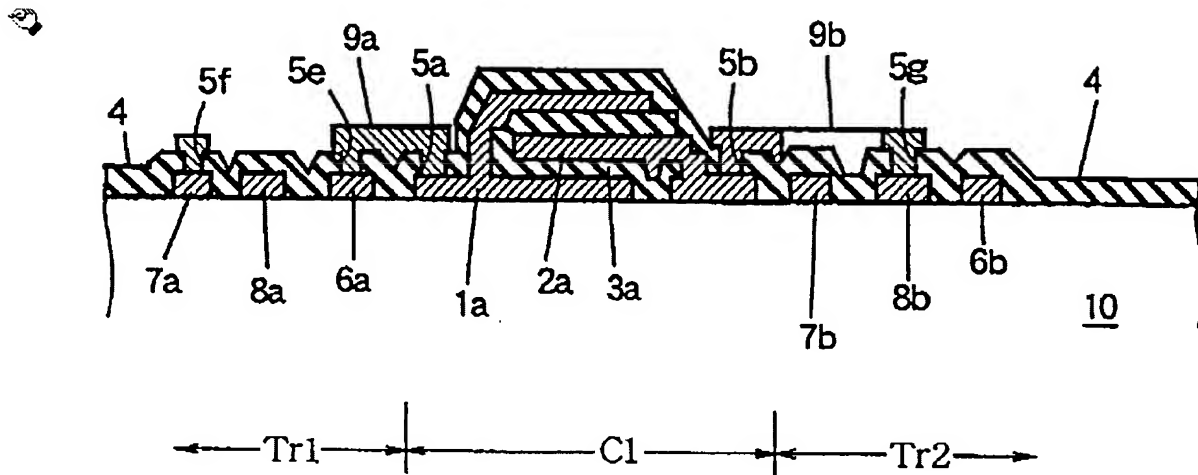
***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2-13 and 19-25, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi.

See reasons of record in the Office action of 25 March 2005.

Figure 1C is copied on the next page:



As noted previously, with respect to claim 4, the "first electrode" is identified as at least a part of the horizontal part of 1a. The "first interconnect" is a horizontal part of 9a. These two features are connected by a conductive path consisting of a vertical region extending through the dielectric layer overlying 1a, which is filled with conductor. This vertical region is identified as the "first via," as required by the third line from the end of the claim. A "first insulating layer" 3a is located over the "first electrode." A "second electrode" is a horizontal part of 2a, which is located over the "first insulating layer." A "second interconnect" is a horizontal feature above 5b. (This feature is identified as 9b in figure 1B and above.) The "second electrode" and the "second interconnect" are connected by a conductive path consisting of three parts: 1) a vertical region extending below electrode 2a (contacting electrode 2a at its right side, and contacting an unnumbered horizontal layer below 5b), 2) the horizontal layer itself below 5b, and 3) a

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vertical region extending below interconnect 9b (contacting the horizontal layer 2) at its right side, and contacting 9b at its left side). Either of the vertical regions 1) or 3) could be identified as the "second via" of the next to last line of the claim (because either of these regions serve to connect the "second electrode" and the "second interconnect" and because the claim is written in open claim language).

There is a "second insulating layer" immediately above the "second electrode" and a "third electrode" immediately above the "second insulating layer." The "third electrode" is connected to the "first interconnect" 9a by a conductive path consisting of three parts: 1) a vertical region extending above 1a, 2) a horizontal region immediately to the left of 1a, and 3) a vertical region extending above 5a. The vertical region 1) is identified as the "third via" of the claim, because it serves to connect the "third electrode" and the "second interconnect," and because the claim is written in open claim language.

Claim 4 is thus anticipated by the reference, and anticipation is the epitome of obviousness. Alternatively, it would have been obvious that the designations of the claim language, such as "electrode" and "interconnect" describe functions of the Hoshi regions.

With respect to claim 19, a "transistor element" is located at, for example, Tr2, with metallization regions shown on the right side of figure 1C. "Substrate" would be read on the part of the semiconductor layer located at least under the transistor. The "dielectric layer" is read on the top dielectric layer shown in the figure, which is identified by a 4 on the right side of the figure. The "first interconnect" 9a is located above this

dielectric layer, coupled to the "first electrode" by a "first via," and to a "second electrode" by a "second via" as set forth above. The "second interconnect" 9b is also above the dielectric layer, and is coupled to the "second electrode" by a "third via" as described above. A "fourth via" is shown below 5g, at the right side of the figure, which couples 9b to transistor Tr2. Claim 19 is anticipated by the reference, and anticipation is the epitome of obviousness. Alternatively, it would have been obvious to one of ordinary skill that the claim language designations identified above describe the functions of the Hoshi regions.

The dependent claims would have been obvious for the reasons identified on page 4 of the previous Office action.

### ***Conclusion***

Applicant's remarks of 22 June 2005 have been considered, but are not convincing. Applicant notes two definitions of the term "via." The first definitions would not seem to apply at all to these claims, because, as noted above, the vertical connections here are not between two interconnects, as required by the definition. The second definition states that, "Openings in the intermetal dielectric layers are known as vias: these allow contact to be made between Metals 1 and 2, Metals 2 and 3, etc." This definition seems to describe exactly the features identified in the Office actions as "vias." Each structure identified as a "via" is in an opening in intermetal dielectric, and allows contact between horizontal metal layers. Applicant alleges in general that there

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are differences in structure and function between the Hoshi structures and such contacts, but there doesn't seem to be any difference in structure or function required by the definition above, or anywhere else in the claim language. The structure is that of a conductor in an opening in a dielectric layer, and the function is to allow for electric contact between overlying and underlying layers. Applicant notes at length differences in processing steps between the invention of Applicant's disclosure and the Hoshi descriptions, but it is not clear why these differences are relevant to patentability. Neither of claims 4 or 19 requires any processing steps at all, and even when specific processes are recited, the burden is on the Applicant to show what structural features necessarily arise from the recited process step, and to show that the prior art does not possess such features. What specific structural feature is Applicant relying upon here to distinguish, required by the claim language and not possessed by the Hoshi device?

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (571) 272-1652.


The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Sara W. Crane  
Primary Examiner  
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